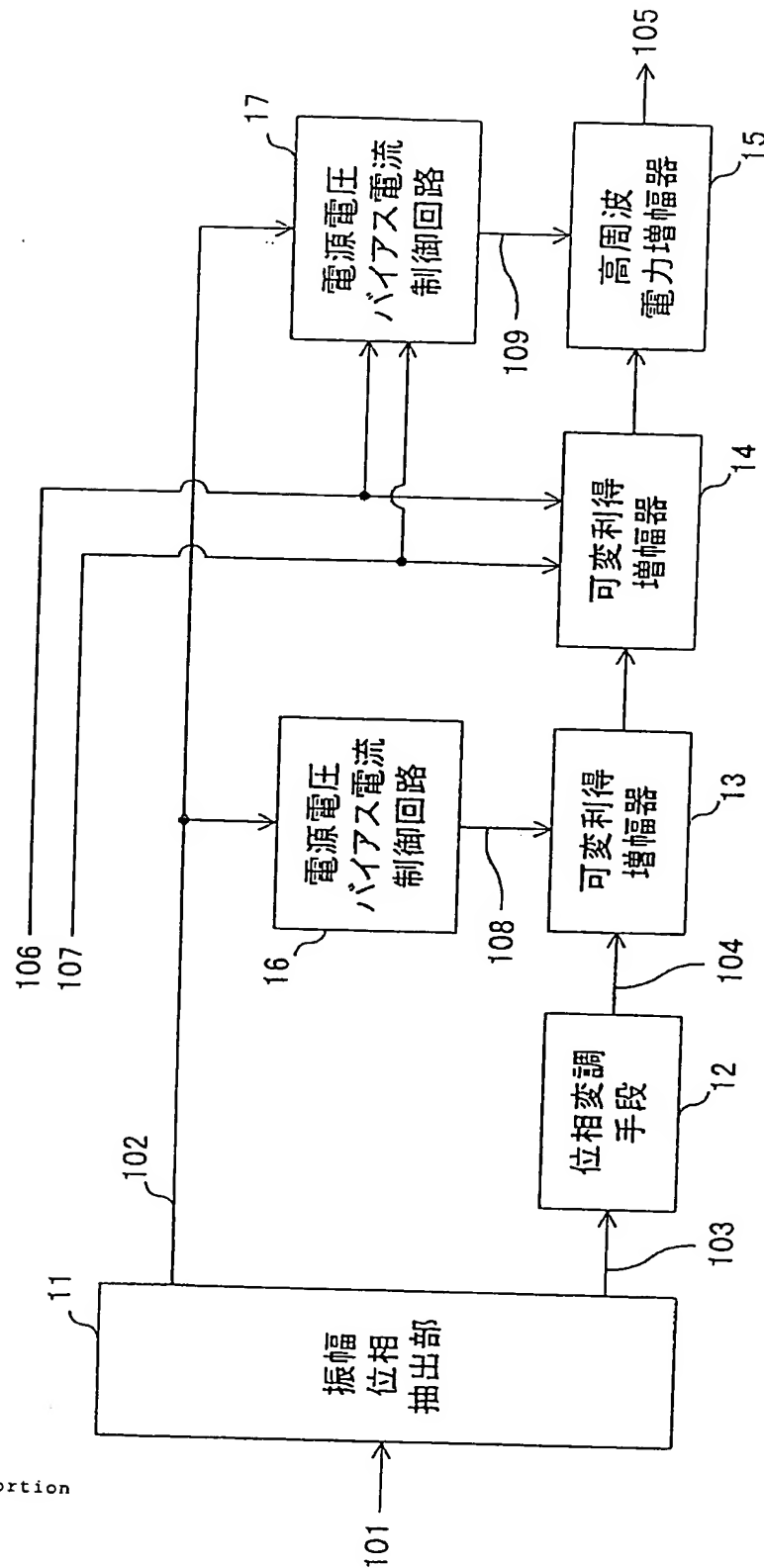
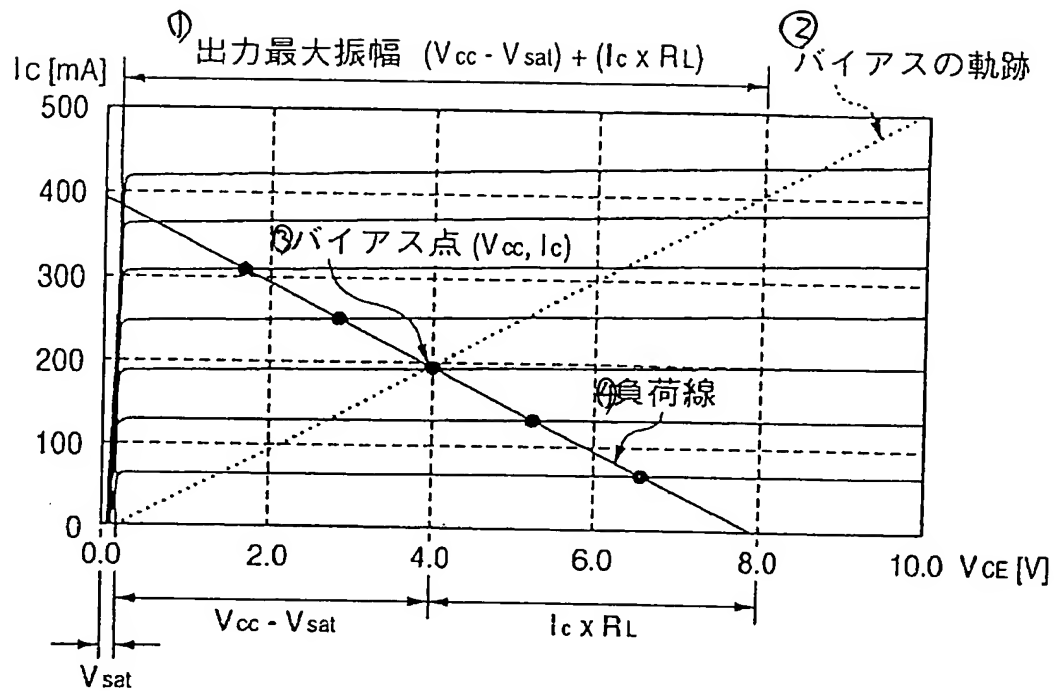


Fig. 1



- 11: amplitude/phase extraction portion
- 12: phase modulation means
- 13: variable gain amplifier
- 14: variable gain amplifier
- 15: high-frequency power amplifier
- 16: supply voltage/bias current control circuit
- 17: supply voltage/bias current control circuit

Fig.2



- ① maximum output amplitude
- ② locus of bias
- ③ bias point
- ④ load line

Fig. 3

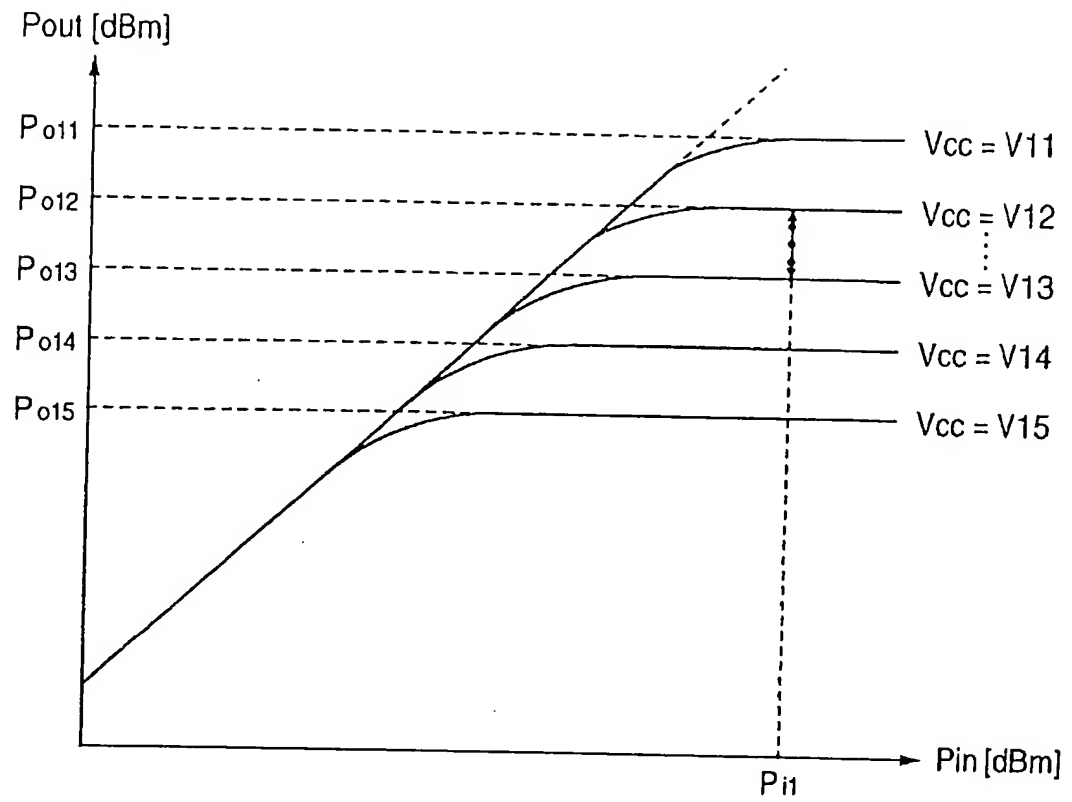


Fig. 4

① time

② linear operating mode

③ gain of variable gain amplifier 14

④ voltage of supply voltage/bias current control circuit 17

⑤ current of supply voltage/bias current control circuit 17

⑥ saturation operating mode

⑦ gain of variable gain amplifier 14

① 時間	② 線形動作モード			⑥ 飽和動作モード		
	可変利得 増幅器14 ③の利得	電源電圧 バイアス電流 制御回路 ④17の電圧	電源電圧 バイアス電流 制御回路 ⑤17の電流	可変利得 増幅器14 ⑦の利得	電源電圧 バイアス電流 制御回路 ⑧17の電圧	電源電圧 バイアス電流 制御回路 ⑨17の電流
t(1,1)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,1)$	$I(1,1)$
t(1,2)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,2)$	$I(1,2)$
t(1,3)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,3)$	$I(1,3)$
t(1,4)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,4)$	$I(1,4)$
t(1,5)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,5)$	$I(1,5)$
t(1,6)	g_1	V_1	I_1	$g_1 + \alpha$	$V(1,6)$	$I(1,6)$
.....
t(n,1)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,1)$	$I(n,1)$
t(n,2)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,2)$	$I(n,2)$
t(n,3)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,3)$	$I(n,3)$
t(n,4)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,4)$	$I(n,4)$
t(n,5)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,5)$	$I(n,5)$
t(n,6)	g_n	V_n	I_n	$g_n + \alpha$	$V(n,6)$	$I(n,6)$
.....

④ voltage of supply voltage/bias current control circuit 17

⑤ current of supply voltage/bias current control circuit 17

Fig. 5

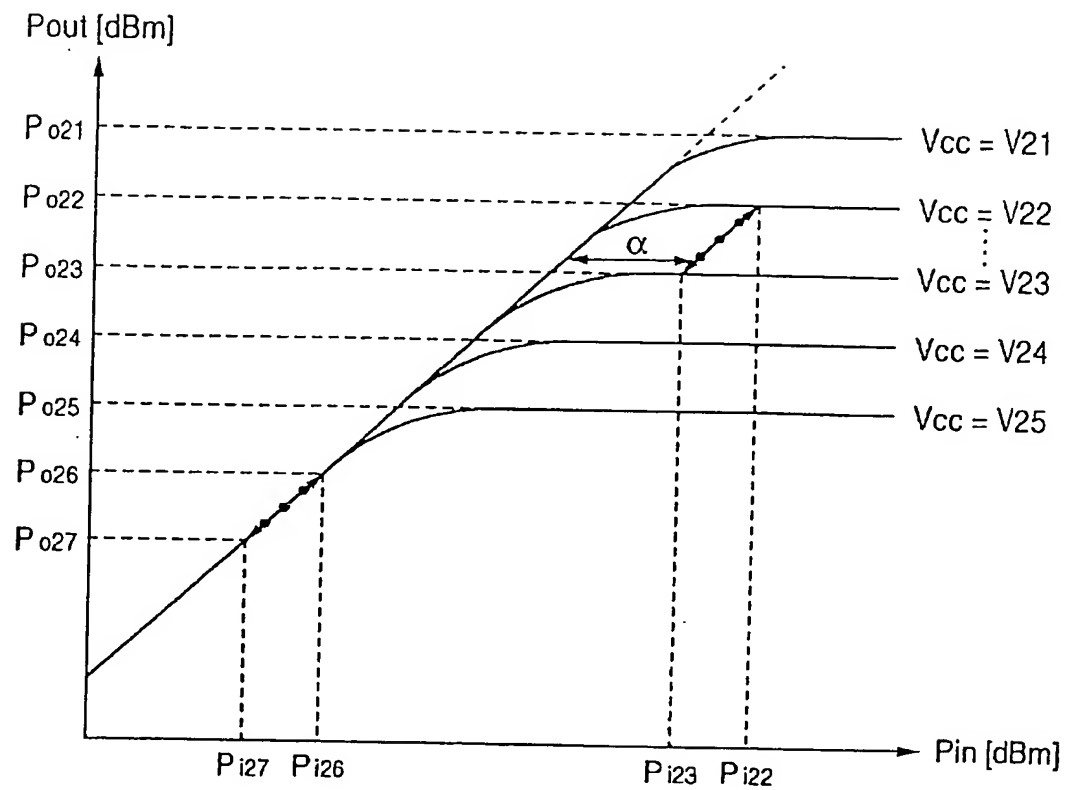


Fig. 6

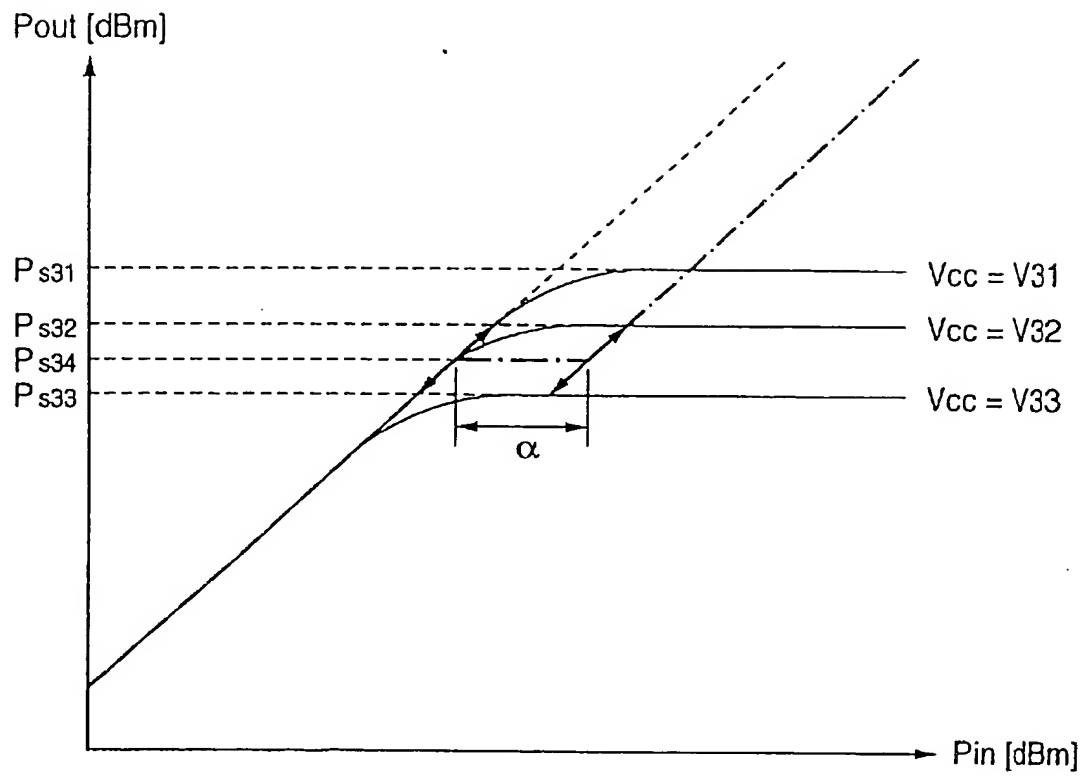


Fig. 7

- 11: amplitude/phase extraction portion
- 12: phase modulation means
- 21: mixer
- 14: variable gain amplifier
- 15: high-frequency power amplifier
- 17: supply voltage/bias current control circuit

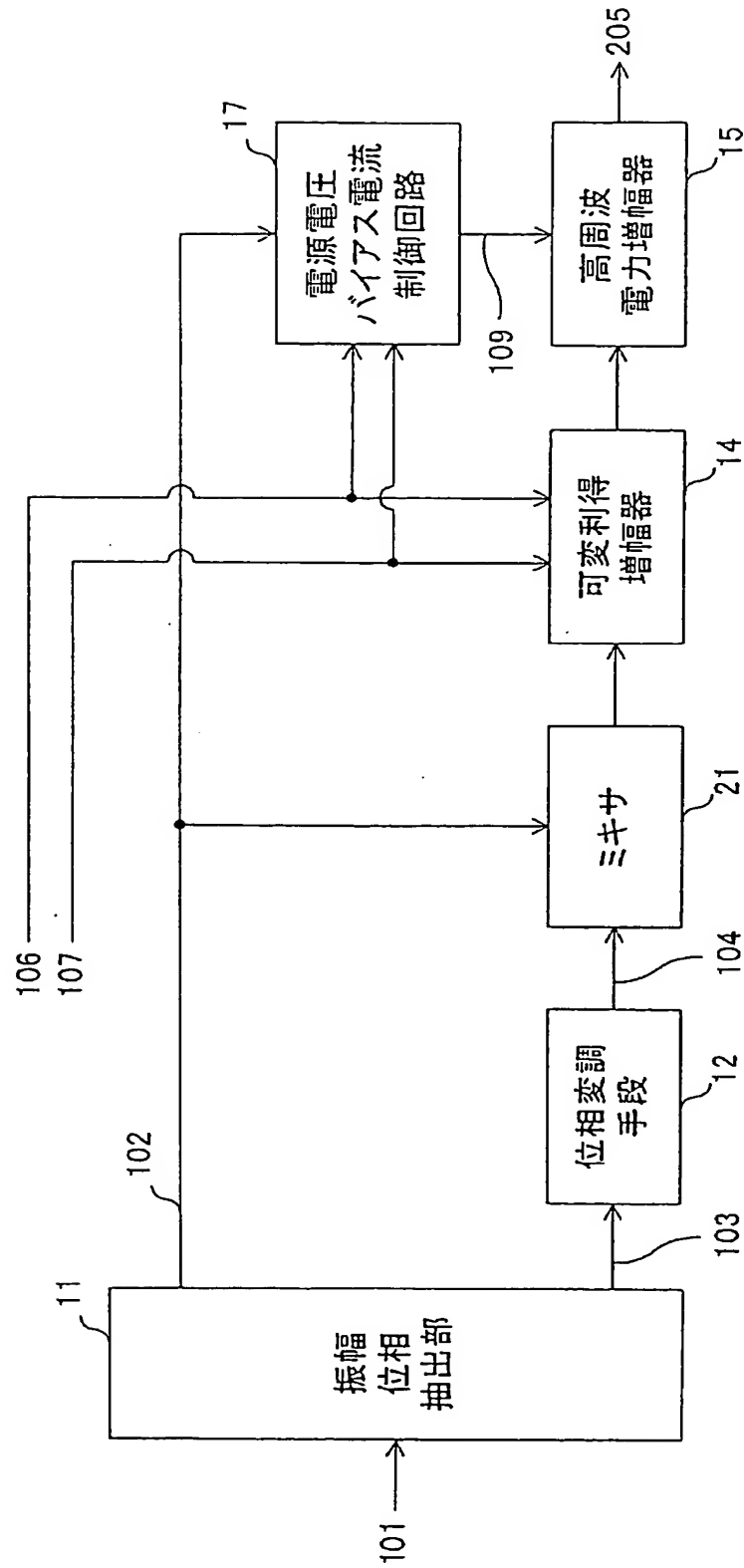


Fig. 8

- 31: amplitude extraction portion
- 32: quadrature modulator
- 14: variable gain amplifier
- 15: high-frequency power amplifier
- 17: supply voltage/bias current control circuit

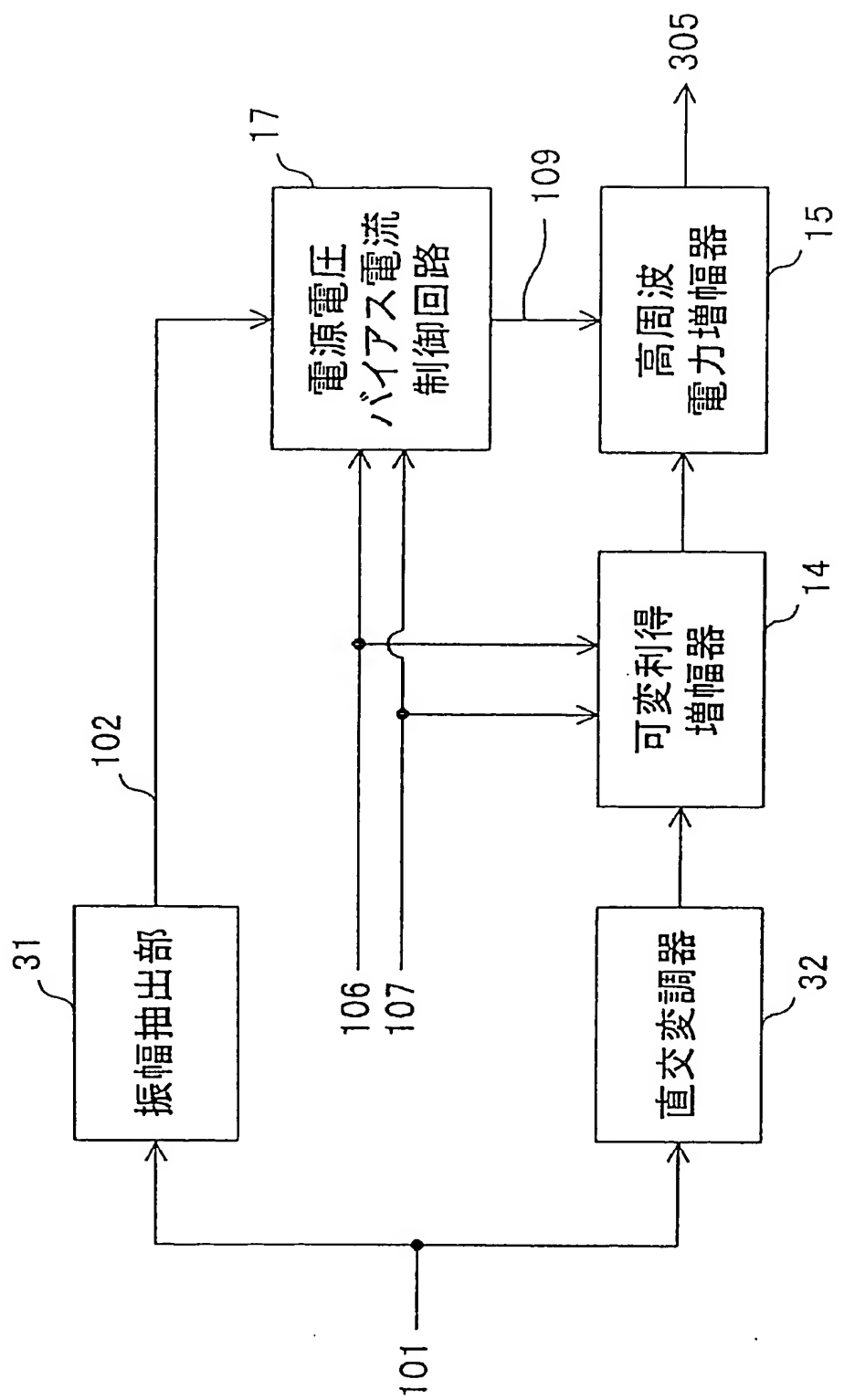


Fig. 9

